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09/191,930	11/13/1998	CHIEN CHIANG	42390.P6459	9178

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EXAMINER

MALSAWMA, LALRINFAMKIM HMAR

ART UNIT	PAPER NUMBER
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2825

DATE MAILED: 11/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/191,930

Applicant(s)

CHIANG ET AL.

Examiner

Lex Malsawma

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 October 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 85-122 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 108-112 is/are allowed.
- 6) ☒ Claim(s) 85-107 and 113-122 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 March 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 85-89 and 102-107 are rejected under 35 U.S.C. 103(a) as being unpatentable over Usami (6,222,269) in view of Havemann (5,751,066) and Doo (4,153,988).

Regarding Claims 85 and 89:

Usami discloses (in Figs. 2A-3C and cols. 5-7) a method of forming an interconnect structure, comprising:

- forming a first layer 4 of a first dielectric material on a substrate;
- patterning the first layer (Fig. 2B);
- depositing conductive material 13 over the patterned first layer;

planarizing the conductive material such that a plurality of interconnect lines 3 are formed including a first and a second “wide” interconnect lines (i.e., note the two interconnect lines “3” on the right side in Fig. 2D) and a third “thin” interconnect line (e.g., the third line being the centrally located “thin” interconnect line “3” among the three “thin” interconnect lines “3” in Fig. 2D);

forming a mask layer 14 over the plurality of interconnect lines 3 and patterned first layer 4 (Fig. 3A);

patterning the mask layer 14 such that the first and second “wide” interconnect lines and a first portion of the patterned first layer 4 are covered, and the third “thin” interconnect line and a second portion of the patterned first layer 4 are uncovered;

removing the second portion of the patterned dielectric material of the first layer 4 from the uncovered portion (Fig. 3B); and

depositing a second layer 5 of a second dielectric material adjacent to the third “thin”, centrally-located interconnect line “3”, the second dielectric material having a smaller dielectric constant than the first dielectric material (Fig. 3C and col. 6, lines 3-9).

Usami **lacks** specifying the plurality of interconnect lines includes power interconnect lines (first and second) and signal interconnect lines (third), however, it is important to note that Usami does not specify whether the interconnect lines “3” may or may not include a combination of power lines and signal lines. Note Usami specifies that a low-dielectric-constant material between signal lines reduces parasitic capacitance and crosstalk (see Usami, col. 8, lines 14-20). Havemann **teaches** a method of forming two different dielectric materials between a plurality of interconnect lines located on the same level of metallization, wherein the method comprises:

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forming a low-dielectric-constant material 34 (note Fig. 3B) between closely-spaced interconnect lines 18 in order to reduce unwanted capacitance between lines 18 (note col. 2, lines 35-37); and forming a “higher” dielectric-constant material 26 between interconnect lines 16 where capacitance is not as critical (note abstract, line 3-5). Doo is **cited only** to show it was very well known in the art that problems associated with power lines (e.g., “driver noise”, note col. 3, lines 51-55) can be reduced by increasing the capacitance of the power line (note col. 4, lines 13-16). The formula for capacitance is well known to any one in the art, and one of ordinary skill in the art would have known that, for a given separation between a pair of formed interconnect lines, the capacitance between the pair can be readily increased or decreased by forming a high-k or low-k dielectric (respectively) in between the pair of interconnect lines. In view of Havemann and Doo, it would have been obvious to one of ordinary skill in the art to modify Usami by utilizing the interconnect lines “3” for a combination of power lines and signal lines on the same level of metallization because the two dielectric materials (“4” and “5”) can be readily utilized to increase capacitance between power lines and to decrease parasitic capacitance between signal lines. *In other words, Usami and Havemann clearly indicate that signal lines will benefit from the low-k material wherein both Usami and Havemann perform dedicated process steps for the very purpose of locating low-k material between interconnect lines that are clearly intended for signal lines; and given the knowledge generally available regarding capacitance of signal lines and power lines (as shown by Doo), one of ordinary skill in the art would have readily recognized that the interconnect lines with the high-k material therebetween are ideal for power lines.* Specifically regarding Claim 89: The cited references are generally applicable to

semiconductor devices; therefore, it would have been obvious to one of ordinary skill in the art to form a microelectronic device utilizing the method of Usami (in view of Havemann and Doo).

Regarding Claim 86:

Usami discloses the second dielectric material 5 comprises SOG having a dielectric constant ($k=3$) that is less than that of silicon dioxide (note col. 7, lines 27-36); and wherein the first dielectric material 4 comprises silicon dioxide.

Regarding Claims 87 and 88:

Usami discloses (in col. 11, lines 36-45) various materials suitable for the second dielectric material. Although Usami does not disclose that the first dielectric material may be of a material having a dielectric constant greater than that of silicon dioxide (i.e., barium strontium titanate "BST"), Havemann discloses various materials other than silicon dioxide may be incorporated as the high-dielectric-constant material (note materials for drawing element "26" in Table 1, cols. 5-6). The cited references disclose the claimed invention except for utilizing BST for the first dielectric material, however, it is noted that BST is/was a very well known high-dielectric-constant material that is/was commonly utilized in the art. Therefore, it would have been obvious to one of ordinary skill in the art to incorporate BST as the high-k material, since it has been held to be within the general skill of a worker in the art to select a known material (i.e., BST) on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Regarding Claims 102-104:

Usami discloses a method of forming an interconnect structure, comprising:

forming on a substrate a first intralayer dielectric 4 and a first plurality of interconnect lines 3 disposed within the first intralayer dielectric 4 (Fig. 2D);

removing a portion of the first intralayer dielectric 4 (Fig. 3B); and

forming a second intralayer dielectric 5 on the substrate where the first intralayer dielectric was removed (Fig. 3C), wherein a dielectric constant of the first intralayer dielectric is different from a dielectric constant of the second intralayer dielectric (the first dielectric is a relatively high-k material and the second dielectric is a low-k material).

Usami **lacks** the following: (1) forming a second plurality of interconnect lines in the second interlayer dielectric, and (2) specifying whether the interconnect lines 3 may or may not include signal lines and power lines. In regards to lacked limitation (1), it is noted Usami discloses forming all conductive lines simultaneously, wherein a plurality of interconnect lines will exist within the second interlayer dielectric layer when said second interlayer dielectric layer is formed. Havemann **teaches** (in Figs. 2A-3B) a method of forming two different dielectric materials between interconnect layer on the same level of metallization, wherein the method can include forming a first plurality of interconnect lines 16 with a first dielectric material between the lines 16, and then forming a second plurality of interconnect lines 18 with a second dielectric material between the lines 18. It is important to note Havemann also teaches (in Figs. 5A-6E) the interconnect lines 16 and 18 may be formed simultaneously instead of forming two pluralities that would require at least two masking/patterning steps, in other words, in view of Havemann, one of ordinary skill in the art would have realized that the interconnect lines of Usami could also be formed in two pluralities, wherein forming two pluralities would require the utilization of at least two masking/patterning steps. In regards to lacked limitation (2), Doo is **cited only** to

show that one of ordinary skill in the art would have realized that the interconnect lines of Usami (or Havemann) are ideal for power lines and signal lines. Doo discloses the well-known problems associated with signal lines and power lines (note col. 3, lines 28-55), wherein problems such as signal propagation delay can be reduced by utilizing a low-dielectric-constant material and problems associated with power lines can be reduced by increasing capacitance of the power lines (note col. 4, lines 13-16), in other words, it was well known in the art to utilize a low-dielectric-constant material between signal lines and to increase the capacitance of power lines in order to effectively decouple noise from the power lines, wherein utilizing a "higher" dielectric-constant material between the power lines is a relatively quick and easy way to increase the capacitance between the power lines. It would have been an obvious matter of design choice for one of ordinary skill in the art to modify Usami by (i) forming two pluralities of interconnect lines instead of simultaneously forming all interconnect lines and (ii) specifying that the interconnect lines comprise signal lines and power lines because of the following reasons: (1) Havemann teaches that either a simultaneous process or two separate patterning processes may be utilized to form interconnect lines on the same level of metallization, and one of ordinary skill in the art would have realized that Usami can also be modified by forming the interconnect lines utilizing two separate patterning processes, wherein one would have realized that two separate patterning processes would increase process time and complexity without any apparent significant benefits, however, one could obviously choose to do so; and (2) the methods disclosed by Usami and Havemann are ideal for acquiring a combination of signal lines and power lines on the same level of metallization, since it was well known in the art (as shown by Doo) that it is desirable to form a low-dielectric-constant material between adjacent signal lines

and that it is desirable to increase the capacitance of power lines (e.g., by incorporating a “higher” dielectric-constant material between adjacent power lines).

Regarding Claim 105:

This claim is similar to Claim 88, therefore, it is held obvious over the cited references with reasoning similar to that applied to Claim 88.

Regarding Claim 106:

In general, the instant claim contains limitations for forming interconnect lines by a damascene process, and although Usami lacks forming a second plurality of interconnect lines, Havemann teaches that interconnect lines on the same level of metallization can be formed by utilizing a simultaneous process or plural processes. The instant claim is held obvious over the cited references because of the following reasons: **(a)** Usami discloses a damascene process, in Figs. 2A-2D, wherein the plurality of conductive lines 3 are formed by etching trenches in the first intralayer dielectric 4, depositing a conductive material 13, and polishing the conductive material such that the conductive material is substantially removed except for that which is in the trenches; **(b)** Usami discloses forming all conductive lines simultaneously using a single damascene process instead of, for example, forming the conductive lines utilizing two separate damascene processes; **(c)** one of ordinary skill in the art would have readily recognized that Usami could be modified, if so desired, by forming several “pluralities” of conductive lines utilizing two or more damascene processes, especially since Havemann teaches interconnect lines on the same level of metallization, having two different dielectrics therebetween, can be formed utilizing a simultaneous process or plural processes; **(d)** forming the conductive lines in several “pluralities” would increase process time and complexity without significant benefits,

however, one could obviously choose to do so if time and cost are not an issue; therefore, if one chooses to form the conductive lines (of Usami) in several "pluralities" (i.e., in a first and second plurality of lines), then it would have been obvious to utilize the process steps in "(a)" when forming each of the several "pluralities" of conductive lines.

Regarding Claim 107:

The cited references are generally applicable to semiconductor devices; therefore, it would have been obvious to one of ordinary skill in the art to form a microelectronic device utilizing the method of Usami (in view of Havemann and Doo).

3. Claims 90-101, 113-122 are rejected under 35 U.S.C. 103(a) as being unpatentable over Havemann (5,751,066) in view of Doo (4,153,988).

Regarding Claims 90, 113-116, 117, 120, and 121:

Havemann discloses a method of forming an interconnect structure, comprising:

forming a first layer of a conductive material (15, 17) on a substrate 12 (Fig. 5A);

forming a first pair of interconnect lines 16 and a second pair of interconnect lines 18 (Fig. 5C);

depositing a first dielectric material 26 over and between the first pair and the second pair (Fig. 5D);

forming a masking layer 50 over the first pair and the second pair and first dielectric material (Fig. 5E and col. 8, lines 26-32);

patterning the mask layer 50 such that one portion of the dielectric material 26 between one pair is covered and another pair is uncovered (Fig. 5E);

removing the portion of the dielectric material that is uncovered (Fig. 6A);
removing the patterned mask layer (Fig. 6B); and
depositing a second dielectric material 34 having a different dielectric constant than a dielectric constant of the first dielectric material 26 where the portion of the dielectric material was removed (Note Table 1; Fig. 6C; and col. 8, lines 36-37), wherein the second material comprises a low-k material and the first material comprises a relatively high-k material (i.e., relatively high in comparison to the second material).

Havemann **lacks** specifically disclosing that lines “16” are for power distribution and that lines “18” are for carrying signals. Doo is **cited only** to show that one of ordinary skill in the art would have readily recognized that the interconnect lines “16” and “18” (of Havemann) are ideal for power lines and signal lines, respectively. Doo discloses the well-known problems associated with signal lines and power lines (note col. 3, lines 28-55), wherein problems such as signal propagation delay can be reduced by utilizing a low-dielectric-constant material and problems associated with power lines can be reduced by increasing capacitance of the power lines (note col. 4, lines 13-16), in other words, it was well known in the art to utilize a low-dielectric-constant material between signal lines and to increase the capacitance of power lines in order to effectively decouple noise from the power lines, wherein utilizing a “higher” dielectric-constant material between the power lines is a relatively quick and easy way to increase the capacitance between the power lines. It would have been obvious to one of ordinary skill in the art to modify Havemann by specifying that interconnect lines “16” and “18” are utilized to distribute power and carry signals, respectively, because the interconnect structure formed by Havemann is ideal for such a utilization. *Specifically regarding Claim 116:* Havemann (in view

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of Doo) discloses the general conditions of the claimed invention except for utilizing BST for the high-dielectric-constant material, however, it is noted that BST is/was a very well known high-dielectric-constant material that is/was commonly utilized in the art. Therefore, it would have been obvious to one of ordinary skill in the art to incorporate BST as the high-k material, since it has been held to be within the general skill of a worker in the art to select a known material (i.e., BST) on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Regarding Claim 96:

Havemann discloses a method of making in-plane decoupling capacitors, comprising:
forming a first plurality of conductive lines 16 on an insulating substrate 12, the first plurality of conductive lines having a first dielectric 26 therebetween (Figs. 1A-2B); and
forming a second plurality of conductive lines 18 on the insulating substrate 12, the second plurality of conductive lines having a second dielectric material 34 therebetween (Figs. 2D-3B);

wherein the first dielectric constant is greater than a dielectric constant of the second dielectric.

Havemann **lacks** specifically disclosing that conductive lines “16” are power lines and that conductive lines “18” are signal lines. Doo is **cited only** to show that one of ordinary skill in the art would have readily recognized that the interconnect lines “16” and “18” (of Havemann) are ideal for power lines and signal lines, respectively. With similar reason applied above, the instant claim is held obvious over the cited references (See above, *Regarding Claims 90 and 113* for detailed reasoning).

Regarding Claims 91-94 and 97-100:

These claims generally contain limitations for a relationship between the dielectric constants of the first and second dielectric materials. Havemann discloses various materials can be utilized for the first and second dielectric materials “26” and “34” (note Table 1, cols. 5-6), wherein materials listed in Table 1 can be readily selected to arrive at the limitations of the current claims. It would have been an obvious matter of design choice for one of ordinary skill in the art to utilize first and second dielectric materials having dielectric constants as specified in the current claims because Havemann discloses a list of materials wherein one can readily choose materials having specific dielectric constants according to design needs. *Specifically regarding Claim 100:* Havemann (in view of Doo) discloses the general conditions of the claimed invention except for utilizing BST for the high-dielectric-constant material, however, it is noted that BST is/was a very well known high-dielectric-constant material that is/was commonly utilized in the art. Therefore, it would have been obvious to one of ordinary skill in the art to incorporate BST as the high-k material, since it has been held to be within the general skill of a worker in the art to select a known material (i.e., BST) on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Regarding Claims 95, 101, and 122:

Havemann (in view of Doo) is generally applicable to semiconductor devices; therefore, it would have been obvious to one of ordinary skill in the art to form a microelectronic device utilizing the method of Havemann (in view of Doo).

Regarding Claims 118 and 119:

These claims contain limitations for forming the low-dielectric-constant material between the signal lines before forming the “higher” dielectric-constant material between the power lines. Given Havemann, one of ordinary skill in the art could have modified the process sequence shown in Figs. 5C-6C with relative ease by performing the following modifications: replacing material “26” with material “34” in the process shown in Fig. 5D; forming/patterning the mask “50” to cover lines “18” instead of lines “16”(in the process shown in Fig. 5E); removing material “34” not covered by mask “50”, i.e., removing material “34” over lines “16” (in the process shown in Fig. 6A); removing the mask “50” (in the process shown in Fig. 6B); and forming material “26” over lines “16” wherein the material “26” would overlap material “34” in the process shown in Fig. 6C. Such a modification would not have required extensive experimentation or research because, in general, the modification would be based on design choice, i.e., based on choosing first to form the low-dielectric-constant material “34” and then patterning the mask “50” accordingly, therefore, the instant claims are held as obvious design choice modifications (of Havemann) that would have been relatively easily performed by one of ordinary skill in the art.

Status of the Claims

4. Claims 1-84 have been canceled.
5. Claims 85-122 are pending.

Allowable Subject Matter

6. Claims 108-112 are allowable over the references of record.

Remarks

7. Claims 108-112 are allowable primarily because the references of record, singly or in combination, cannot anticipate or fairly suggest the process specified in Claim 108, wherein the process requires forming the second dielectric layer where the portion of the first dielectric layer was removed, followed by forming signal lines in the first dielectric layer and a power line in the second dielectric layer (i.e., note the embodiment shown in Figs. 17-21).

8. Applicants' remarks/arguments have been carefully reviewed and considered, but they are generally not persuasive with respect to Claims 85-107 and 113-122. Applicants maintain that the combinations of references (Havemann, Doo, and/or Usami) do not teach or suggest the claimed invention, especially since *"it is not known to reduce driver noise of power lines and reduce parasitic capacitance of signal lines in a given interconnect level by depositing a different dielectric material next to a signal interconnect line than a dielectric material having patterned therein power interconnect lines"* (note remarks on page 14, 3rd paragraph). As stated in the prior Office action, the Examiner maintains his position that the current invention is held obvious over the cited reference primarily because Usami and/or Havemann disclose all significant aspects of the current claims, and the only significant modification to Usami and/or Havemann, necessary to arrive at the current invention, is for one of ordinary skill in the art to realized that the interconnect lines (in Usami and/or Havemann) can be used for distribution of power and signals. In other words, no significant modification of Usami and/or Havemann is necessary to arrive at the current invention, but rather, one only needs to realize that the interconnect lines can function as power lines and signal lines. Since Applicants acknowledge it

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is well known in the art that interconnect lines are generally used to distribute power and signals (note specification, page 6, lines 11-21), one of ordinary skill in the art would have realized that the interconnect lines of Usami and/or Havemann can be used for power lines and signal lines; furthermore, Applicants admit that the concept of capacitance is also very well known such that one of ordinary skill in the art would have clearly realized that the interconnect lines having the high-k material therebetween (i.e., the "high-k interconnect lines") are ideal for power lines, especially since both Usami and Havemann perform intricate/dedicated process steps for the very purpose of forming "low-k interconnect lines" and "high-k interconnect lines" on the same level of metallization, wherein the "low-k interconnect lines" are clearly for signal lines.

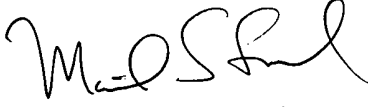
9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lex Malsawma whose telephone number is 703-306-5986. The examiner can normally be reached on Monday-Thursday and Saturday 1 PM - 9:30 PM (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 703-308-1323. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Lex Malsawma 

October 29, 2003


MATTHEW SMITH
SUPERVISOR
TECHNOLOGY CENTER 2800